## AMENDMENTS TO THE CLAIMS

1-20. (Canceled)

21. (Currently Amended) A pulse generator circuit for generating an input signal for a flip flop circuit from a clock signal and from a data signal, comprising:

a clock pulse field effect transistor, at the gate terminal of which the clock signal ~~can be~~is applied and at the first source/drain terminal of which the input signal for ~~a~~ the flip flop circuit ~~can be~~is provided;

a logic field effect transistor, at the gate terminal of which the data signal ~~can be~~is applied and the first source/drain terminal of which is coupled to the second source/drain terminal of the clock pulse field effect transistor;

a feedback field effect transistor, at the gate terminal of which a feedback signal based on the clock signal ~~can be~~is applied, the first source/drain terminal of which is coupled to the second source/drain terminal of the logic field effect transistor and at the second source/drain terminal of which a first electrical reference potential ~~can be~~is applied; and

a control unit configured to control the clock pulse field effect transistor, the logic field effect transistor and the feedback field effect transistor such that, to generate the input signal, the clock pulse field effect transistor is chronologically activated after the logic field effect transistor and the feedback field effect transistor ~~to generate a flip flop signal~~are activated.

22. (Currently Amended) The pulse generator circuit as claimed in claim 21, further comprising an additional clock pulse field effect transistor, at the gate terminal of which the clock signal ~~can be~~is applied, at the first source/drain terminal of which a second electrical reference potential ~~can be~~is applied, and the second source/drain terminal of which is coupled to the first source/drain terminal of the clock pulse field effect transistor.

23. (Currently Amended) The pulse generator circuit as claimed in claim 22, further comprising an additional feedback field effect transistor, the gate terminal of which is coupled to the gate

terminal of the feedback field effect transistor, at the first source/drain terminal of which the second electrical reference potential ~~can be~~is applied, and the second source/drain terminal of which is coupled to the first source/drain terminal of the clock pulse field effect transistor.

24. (Currently Amended) The pulse generator circuit as claimed in claim 21, comprising a bypass field effect transistor, the gate terminal of which is coupled to the flip flop circuit, at the first source/drain terminal of which the first electrical reference potential ~~can be~~is applied, and the second source/drain terminal of which is coupled to the second source/drain terminal of the clock pulse field effect transistor.

25. (Canceled)

26. (Previously Presented) The pulse generator circuit as claimed in claim 22, wherein the first electrical reference potential is an electrical ground potential and/or wherein the second electrical reference potential is an electrical supply potential.

27. (Previously Presented) The pulse generator circuit as claimed in claim 21, wherein the clock pulse field effect transistor, the logic field effect transistor and the feedback field effect transistor are field effect transistors of the n-type of conduction.

28. (Previously Presented) The pulse generator circuit as claimed in claim 23, wherein the additional clock pulse field effect transistor and the additional feedback field effect transistor are field effect transistors of the p-type of conduction.

29. (Previously Presented) The pulse generator circuit as claimed in claim 24, wherein the bypass field effect transistor is a field effect transistor of the n-type of conduction.

30. (Currently Amended) The pulse generator circuit as claimed in claim 21, wherein the clock pulse field effect transistor, the logic field effect transistor, and the feedback field effect transistor

form a first signal path, and

wherein the pulse generator circuit further comprises a second signal path ~~of additional field effect transistors which has the same circuit~~having a complementary clock pulse field effect transistor, a complementary logic field effect transistor, and a complementary feedback field effect transistor which are interconnected in a same way as the clock pulse field effect transistor, the logic field effect transistor, and the feedback field effect transistor of the first signal path, and the complementary clock pulse field effect transistor, the complementary logic field effect transistor, and the complementary feedback field effect transistor~~additional field effect transistors~~ are interconnected for generating from the clock signal and from a complementary data signal which is complementary to the data signal a complementary input signal which is complementary to the input signal for the flip flop circuit.

31. (Previously Presented) The pulse generator circuit as claimed in claim 30, wherein the first source/drain terminal of the additional clock pulse field effect transistor of the second signal path is coupled to the gate terminal of the additional feedback field effect transistor of the first data path.

32. (Previously Presented) The pulse generator circuit as claimed in claim 30, wherein the first source/drain terminal of the clock pulse field effect transistor of the first signal path is coupled to the gate terminal of the additional feedback field effect transistor of the second data path.

33. (Previously Presented) The pulse generator circuit as claimed in claim 21, wherein the control unit is configured to apply the data signal to the gate terminal of the logic field effect transistor chronologically before the clock signal is switched to change the clock pulse field effect transistor from a state with nonconducting channel region into a state with conducting channel region.

34. (Currently Amended) A circuit arrangement, comprising:

a pulse generator circuit as claimed in claim ~~30; and~~21,

~~a~~ wherein the flip flop circuit, which is interconnected with the pulse generator circuit such

that the input signal which ~~can be~~is generated by the pulse generator circuit ~~can be~~is coupled into the flip flop circuit.

35. (Currently Amended) The circuit arrangement as claimed in claim 34, wherein the flip flop circuit has storage field effect transistors configured to store a storage signal based on at least one of the input signal ~~and/or~~and the complementary input signal.

36. (Previously Presented) The circuit arrangement as claimed in claim 35, wherein the flip flop circuit comprises switching field effect transistors which are connected between the storage field effect transistors and the pulse generator circuit.

37. (Currently Amended) The circuit arrangement as claimed in claim 36, ~~further comprising~~wherein the switching field effect transistors comprise a first switching field effect transistor, the gate terminal of which is coupled to the first source/drain terminal of the clock pulse field effect transistor, at the first source/drain terminal of which the second electrical reference potential ~~can be~~is applied, and the second source/drain terminal of which is coupled to a storage node of the storage field effect transistors.

38. (Currently Amended) The circuit arrangement as claimed in claim 37, wherein the switching field effect transistors comprise~~further comprising~~ a second switching field effect transistor, the gate terminal of which is coupled to ~~the~~ a gate terminal of ~~the~~ a complementary bypass field effect transistor, at the first source/drain terminal of which the first electrical reference potential ~~can be~~is applied, and the second source/drain terminal of which is coupled to the second source/drain terminal of the first switching field effect transistor.

39. (Currently Amended) The circuit arrangement as claimed in claim 38, ~~further comprising~~wherein the flip flop circuit comprises a protective field effect transistor, the gate terminal of which is coupled to the gate terminal of the first switching field effect transistor, the first source/drain terminal of which is coupled to the second source/drain terminal of the first switching

field effect transistor and to a source/drain terminal of a storage field effect transistor, and the second source/drain terminal of which is coupled to a source/drain terminal of another storage field effect transistor.

40. (Currently Amended) The circuit arrangement as claimed in claim ~~34~~35, wherein the flip flop circuit has complementary storage field effect transistors configured~~further comprising a fourth signal path of additional field effect transistors, which has the same circuit as a third signal path formed from the field effect transistors of the flip flop circuit, which additional field effect transistors of the flip flop circuit are interconnected~~ to store a complementary storage signal which is complementary to the storage signal.

41. (Currently Amended) A circuit arrangement, comprising:

a pulse generator means for generating an input signal for a flip flop circuit from a clock signal and from a data signal, comprising:

a clock pulse field effect transistor, at the gate terminal of which the clock signal ~~can be~~is applied and at the first source/drain terminal of which the input signal for a flip flop circuit ~~can be~~is provided;

a logic field effect transistor, at the gate terminal of which the data signal ~~can be~~is applied and the first source/drain terminal of which is coupled to the second source/drain terminal of the clock pulse field effect transistor;

a feedback field effect transistor, at the gate terminal of which a feedback signal based on the clock signal ~~can be~~is applied, the first source/drain terminal of which is coupled to the second source/drain terminal of the logic field effect transistor and at the second source/drain terminal of which a first electrical reference potential ~~can be~~is applied; and

a control means for controlling the clock pulse field effect transistor, the logic field effect transistor and the feedback field effect transistor such that, to generate the input signal, the clock pulse field effect transistor is chronologically activated after the logic field effect transistor and the feedback field effect transistor ~~to generate a flip flop signal~~are activated,

wherein the flip flop circuit is interconnected with the pulse generator means such that the

input signal which ~~can be~~is generated by the pulse generator circuit ~~can be~~is coupled into the flip flop circuit.

42. (Currently Amended) A pulse generator circuit for generating an input signal for a flip flop circuit from a clock signal and from a data signal, comprising:

a clock pulse field effect transistor;

a logic field effect transistor;

a feedback field effect transistor; and

a control unit configured to control the clock pulse field effect transistor, the logic field effect transistor and the feedback field effect transistor such that, to generate the input signal, the clock pulse field effect transistor is chronologically activated after the logic field effect transistor and the feedback field effect transistor ~~to generate a flip flop signal~~are activated.

43. (Currently Amended) A pulse generator circuit for generating an input signal for a flip flop circuit from a clock signal and from a data signal, comprising:

a clock pulse field effect transistor;

a logic field effect transistor;

a feedback field effect transistor; and

a control means for controlling the clock pulse field effect transistor, the logic field effect transistor and the feedback field effect transistor such that, to generate the input signal, the clock pulse field effect transistor is chronologically activated after the logic field effect transistor and the feedback field effect transistor ~~to generate a flip flop signal~~are activated.